CLAIMS

What is claimed is:

1. An apparatus comprising:

a slave access circuit coupled to one of P slave devices and K slave buses to provide access to the one of the P slave devices from one of N master processors via a system bus controller, the K slave buses being configured to couple to the P slave devices, the system bus controller dynamically mapping address spaces of the P slave devices; and

a slave bus decoder coupled to the slave access circuit to enable the one of the P slave devices to connect to one of the K slave buses when the one of the P slave devices is addressed by the one of the N master processors, the slave bus decoder being controlled by the system bus controller.

2. The apparatus of claim 1 wherein the slave access circuit comprises:

K bus buffers coupled to the K slave buses to buffer bus signals corresponding to access signals to the one of the P slave devices, the K bus buffers being enabled by the slave bus decoder.

3. The apparatus of claim 2 wherein each of the K bus buffers is connected to each of the K slave buses.

4. An apparatus comprising:

an arbiter to arbitrate access requests from N master processors via N master buses, the arbiter generating arbitration signals;

a mapping circuit to store mapping information to dynamically map an address space of P slave devices coupled to K slave buses based on the arbitration signals; and

a switching circuit coupled to the arbiter and the mapping circuit to connect the N master buses to K slave buses based on the arbitration signals and the mapping information.

5. The apparatus of claim 4 further comprising:

a slave access decoder coupled to the arbiter and the N master processors to decode addresses issued by the N master processors, the slave access decoder generating control signals to P slave interface circuits, each of the P slave interface circuits being connected to each of the P slave devices.

6. The apparatus of claim 5 wherein the mapping information is provided by a supervisor processor.

7. The apparatus of claim 4 wherein the mapping information is accessible to the N master processors.

8. A method comprising:

providing access to one of the P slave devices from one of N master processors via a system bus controller and K slave buses, the K slave buses being configured to couple to the P slave devices;

dynamically mapping address spaces of the P slave devices by the bus controller;

enabling the one of the P slave devices to connect to one of the K slave buses by a slave bus decoder when the one of the P slave devices is addressed by the one of the N master processors; and

controlling the slave bus decoder by the system bus controller.

9. The method of claim 8 wherein providing access comprises:

buffering bus signals corresponding to access signals to the one of the P slave devices by K bus buffers; and

enabling the K bus buffers by the slave bus decoder.

10. The method of claim 9 wherein buffering the bus signals comprises:

connecting each of the K bus buffers to each of the K slave buses.

11. An method comprising:

arbitrating access requests from N master processors via N master buses by an arbiter, the arbiter generating arbitration signals;

storing mapping information in a mapping circuit to dynamically map an address space of P slave devices coupled to K slave buses based on the arbitration signals; and

connecting the N master buses to K slave buses based on the arbitration signals and the mapping information.

12. The method of claim 11 further comprising:

decoding addresses issued by the N master processors by a slave access decoder;

generating control signals to P slave interface circuits by the slave access decoder, each of the P slave interface circuits being connected to each of the P slave devices.

13. The method of claim 12 wherein the mapping information is provided by a supervisor processor.

14. The method of claim 11 wherein the mapping information is accessible to the N master processors.

15. A system comprising:

a bus controller coupled to N bus masters and K slave buses;

P slave devices; and

P slave interface circuits coupled to the P slave devices and the K slave buses, each of the P slave interface circuits comprising:

a slave access circuit coupled to one of the P slave devices and the K slave buses to provide access to the one of the P slave devices from one of the N master processors via the system bus controller, the K slave buses being configured to couple to the P slave devices, the system bus controller dynamically mapping address spaces of the P slave devices, and

a slave bus decoder coupled to the slave access circuit to enable the one of the P slave devices to connect to one of the K slave buses when the one of the P slave devices is addressed by the one of the N master processors, the slave bus decoder being controlled by the system bus controller.

16. The system of claim 15 wherein the slave access circuit comprises:

K bus buffers coupled to the K slave buses to buffer bus signals corresponding to access signals to the one of the P slave devices, the K bus buffers being enabled by the slave bus decoder.

17. The system of claim 16 wherein each of the K bus buffers is connected to each of the K slave buses.

18. A system comprising:

N bus masters having N master buses;

P slave devices coupled to K slave buses; and

A system bus controller coupled to the N bus masters and the K slave buses, the bus controller comprising:

an arbiter to arbitrate access requests from the N master processors via the N master buses, the arbiter generating arbitration signals,

a mapping circuit to store mapping information to dynamically map an address space of P slave devices coupled to K slave buses based on the arbitration signals, and

a switching circuit coupled to the arbiter and the mapping circuit to connect the N master buses to K slave buses based on the arbitration signals and the mapping information.

19. The system of claim 18 wherein the system bus controller further comprising:

a slave access decoder coupled to the arbiter and the N master processors to decode addresses issued by the N master processors, the slave access decoder generating control signals to P slave interface circuits, each of the P slave interface circuits being connected to each of the P slave devices.

20. The system of claim 19 wherein the mapping information is provided by a supervisor processor.

21. The system of claim 18 wherein the mapping information is accessible to the N master processors.